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68K ColdFire® MICROPROCESSORS

Application Note

Evaluating ColdFire in a 68K Target System: MC68340 Gateway Reference Design

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Motorola's 68K family has been the market leader in embedded applications for many years. As a result of this, there is a great wealth of experience in the industry surrounding the architecture. The highly competitive nature of the embedded systems market compels designers to strive to find the best trade-off between price and performance for microprocessors. Methods used by microprocessor manufacturers to improve processor performance such as pipelining or increasing on-chip cache can be very expensive with respect to silicon area. To overcome this problem and minimize cost with maximum performance, it may be necessary to implement changes in the architecture. This can result in difficulties when a designer wishes to upgrade their design. There may be implications for hardware and software compatibility which would not be present if the architecture remained unmodified.

The ColdFire® architecture has been designed specifically for high performance, cost sensitive embedded applications. In doing this, the 68K architecture was analysed and the way that embedded systems designers use the architecture was examined. As a result, the features of the architecture used less frequently in embedded system design were removed.

Digital DNA From Motorola

The ColdFire architectures' foundation in Motorola's 68000 architecture allows designers to take advantage of the established tool support, code evolution, and engineering expertise. It uses a variable length RISC instruction set to optimize both code density and allow one instruction to be issued every clock cycle where possible. The ColdFire instruction set is a subset of the 68K instruction set, that is compatible at both assembler and binary levels. The programming model is also identical to the 68K, with the exception that it has a simplified stack pointer and exception stack frame.

The Gateway reference design which will be discussed is an integrated circuit board which will bridge an existing MC68340 system to the ColdFire MCF5206 microprocessor, to evaluate the ease of upgrading to a higher performance architecture. It can be used to evaluate system enhancements such as on-chip instruction and/or data cache and bursting to external memory. It can also be used to port a customer’s system code to the ColdFire architecture in situ as opposed to the traditional method of initially porting code to an evaluation platform. This paper is intended to describe the use and operation of the Gateway board.

In using the Gateway solution, the 68K processor initialisation code has to be configured to run on the internal register map of the ColdFire processor. Although the ColdFire architecture is derived from the 680x0 family with a simplified set of instructions and addressing modes, assembler programs while straightforward to port to ColdFire may require some modification before they will run. To help customers with this translation process, Motorola has funded the development of an assembler code converter - PortASM/68K, written by MicroAPL Ltd. in the U.K.

(Consult http://www.mot.com/SPS/HPESD/tools/companion.html for more information on this tool.)

This utility will run on either PC’s (under DOS, Windows 3.x, Windows95/98 & Windows NT) or Sun Workstations (under SunOS or Solaris) and is available free of charge via download from the web.

This converter not only converts the 68K assembler code to ColdFire assembler but analyses how the original code operates allowing the analyser to produce optimized ColdFire code in two passes, rather than just a straight translation.

1.1 Design Considerations

There are two important differences between the ColdFire MCF5206 Microprocessor and MCF68340. The first is the absence of DMA functionality and the second is the lack of an extra 8-bit GPIO port on the ColdFire device. MCF5206 only has one eight bit port that is multiplexed with the PST and DDATA debug signals used for the background debug mode port (BDM). The MC68340 has two dedicated I/O ports, Port A and Port B. Hence, the Gateway hardware must create an additional I/O port and 2 channel DMA module to emulate the MC68340 functionality.

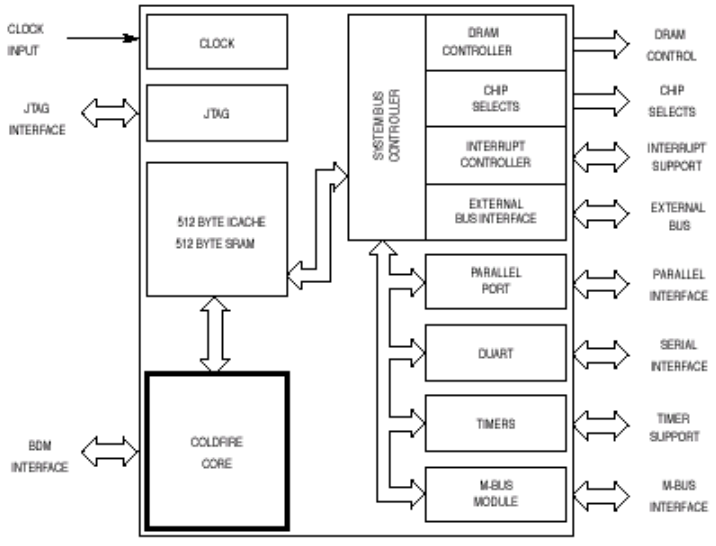

Figure 1. MCF5206 Block Diagram

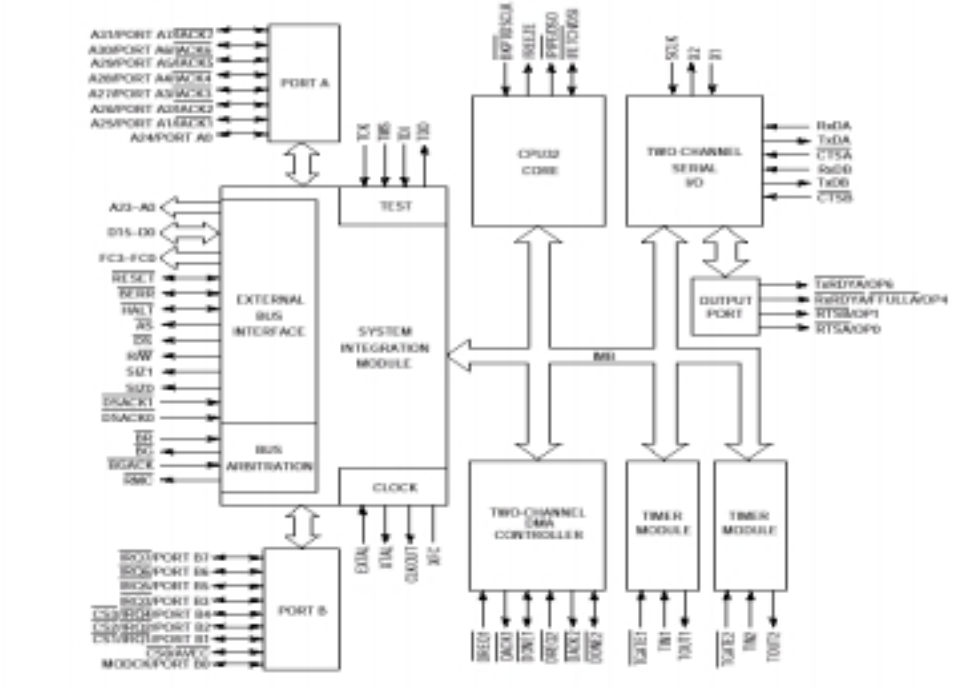

Figure 2. MC68340 Block Diagram

A key feature required for debugging a microprocessor system is memory. This allows the designer to download and run code. The ColdFire MCF5206 microprocessor has 512 bytes of on-chip Static RAM (SRAM) and a DRAM control module built onto the silicon from which external memory can be “gluelessly” interfaced. The DRAM controller offers the designer a clear cost saving by reducing the component count of the system. This module also provides the flexibility to interface to multiple memory configurations.

In addition to requiring DRAM or SRAM memory for debugging software, many designers require non-volatile storage in the form of FLASH memory to store boot code or data that has been collected by the system. Data or code stored in FLASH memory can be accessed, modified or erased via the BDM port.

With this in mind, the MC68340 to MCF5206 Gateway Reference Module was designed with 1 Mbyte of EDO DRAM, 1 Mbyte FLASH ROM, 1 additional 8-bit I/O port and a two channel DMA controller. It consists of two boards, an interconnect board that will connect to the 68K target and a microprocessor / memory board which contains the ColdFire device. This second board provides additional hardware performing many tasks such as control processing from external hardware, pulling active low control signals to a high logic level and decoupling all power supplies to suppress noise. Given the modules incorporated into the design, the reference module can be considered a self-contained ColdFire sub-system.

1.2 MC68340 PGA–MCF5206FT, Gateway Reference Design

1.2.1 MCF5206 CPU, DMA Controller, RESET and Clock Circuit

Figure 4 shows the circuit diagram of the 2-channel DMA controller with the MCF5206 microprocessor. The logic for the DMA controller was implemented using a Motorola MC92310CE ASIC specifically designed for this function

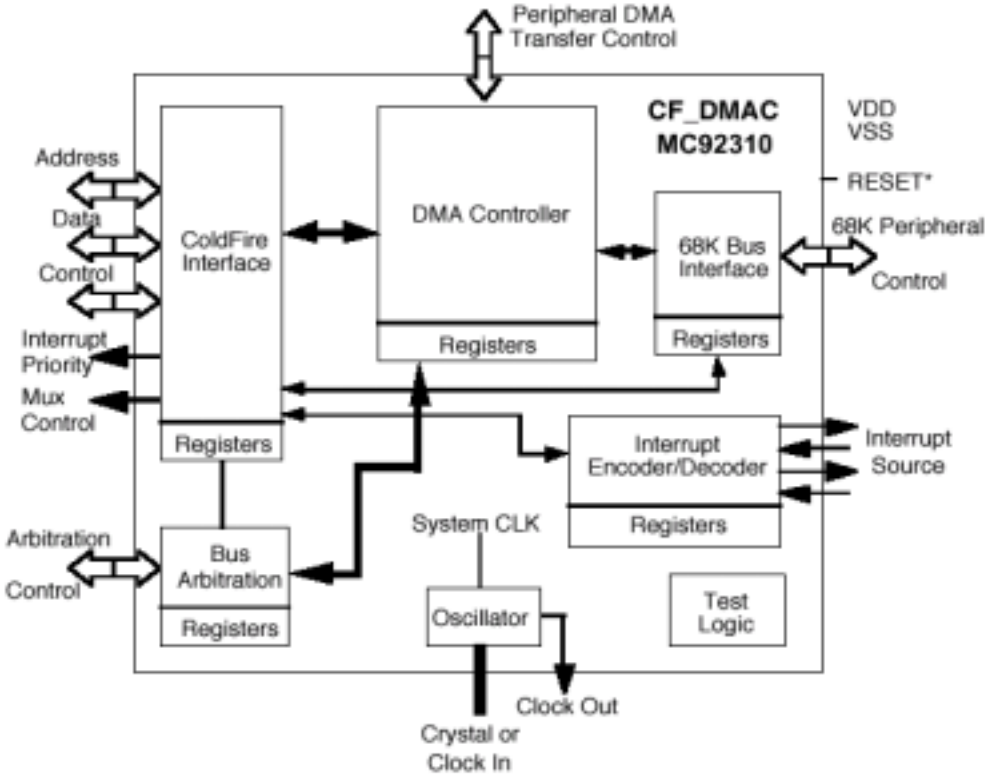

Figure 3. MC92310 Block Diagram

1.2.1.1 Clock Circuit

The clock supply to both the MCF5206 microprocessor and MC92310 dual channel DMA ASIC is selectable via jumper JP3. The clock source can be from either a 25MHz oscillator (SMT), (jumper position 1 / 2), or the CLKIN input pin connected to an external source on the target hardware, (jumper position 2 / 3).

1.2.1.2 Reset Circuit

The main reset signal, RSTI, is controlled by the MAX7705CSA chip shown in Figure 4. This chip provides the circuit with power-supply glitch immunity and guaranteed power-on reset delay whilst continually monitoring the power supply to the microprocessor. The added advantage of using this type of device is that it requires no additional discrete components. The chip is powered by a 5V supply and is activated by bridging the RESET jumper, JP2. The RESET line is pulled up to a logic high level via a 4.7K resistor (R37). The RESET signal is jumper selectable to allow the target hardware to reset the MCF5206 if required.

1.2.1.3 Direct Memory Access Controller (DMA)

An ASIC has been designed to provide the functionality of the MC68340 DMA controller with a ColdFire interface.

Address (A1–A23) and data lines (D0–31) from the MCF5206 Microprocessor connect directly to the ASIC. On board power-up, the physical transfer size of data through the DMA can be set. Data can be transferred in words (16 bit) or long words (32 bit).

/SIZE pin	logic 0	jumper in 2 / 1 position	word size
	logic 1	jumper in 3 / 2 position	long-word size

The chip select for the dual DMA controller is generated by chip select 5 (CS5) on the MCF5206. Chip selects 2,3 and 6 on the MCF5206 are connected to chip selects 1,2 and 3 on the MC68340 target hardware and re-routed via the routing PCB. Timing differences on the chip select lines due to different processor speeds and peripheral access times must be considered and accounted for in the ColdFire initialisation code, usually by the addition of programmable wait states. To make use of the full debug capabilities of the MCF5206, a 26-way BDM connector has been included on the Gateway Reference Board. A designer can download, debug, step and trace their code, and program the flash

1.2.1.4 Pull-Up Resistors, LED's and Miscellaneous Connections

The green surface mount LED, D2, is connected to the 5V supply and current limited by the 1K resistor, R1. This indicates that power is applied to the Gateway board. The red LED, D1 indicates that a RESET signal has been asserted either by the reset controller, the MC68340 target hardware or by an external device through the BDM target connector. GPIO activity on the debug DDATA port pins is indicated using three different colored LED's – D3, D4 and D5 (Red, yellow and green respectively). These LEDs may also be driven by customer firmware, if required.

All critical active low control signals must be pulled high to avoid false signals and erroneous switching. These key control signals and their appropriate pull-up resistance values are shown at the bottom of Figure 4 and Figure 10.

1.2.2 Additional 8 Bit I/O Interface for The MCF5206

The schematic in Figure 4 shows how the additional 8-bit I/O port is created using a Motorola MC74AC646DW. This device provides multiplexed transmission of data directly from the data bus to and from the MCF5206. The MC74AC646DW has internal registers which give the port an additional feature in that data can be stored and clocked out of the port. This feature can be activated by pulling JP6 or JP7 high.

Chip select 7 from the MCF5206 will enable the additional port. The Read/Write (R/W) line from the MCF5206 determines whether the port is an input or an output and is connected to the output enable direction (DIR) pin. If this line is driven low the port will act as an output for a write and conversely a high will configure the port as an input for a read.

In order to activate, or address the 8-bit I/O interface, the active low chip enable pin on the MC74AC646 chip must be driven low. Chip select 7 from the MCF5206 Microprocessor carries out this function. Since the control signal for chip enable is active low, pull-up resistor R39 is required for correct circuit operation at power up.

The MC74AC646DW uses the same clock signal as the MCF5206 ensuring that the additional I/O port operates synchronously.

1.2.3 MC68340 PGA Connector/PGA Footprint

The diagram in Figure 6 shows the connections from the MC68340 Plastic Grid Array (PGA) to four 36-way SMT connectors. For reference, the diagram in Figure 7 shows the footprint (bottom view) of the MC68340 Microprocessor (Each line on Figure 6 is labeled to its reference on the footprint of the MC68340 in Figure 7).

The initial target for this Gateway design was a MC68340 in a PGA package. With the use of an adapter, this reference design has also been used to target a MC68340 in a PQFP package in a customers target system.

1.2.4 PAL Logic for Bus Arbitration & FLASH Control

As previously discussed, the Gateway reference design has FLASH memory on the board. Additional logic is required to interface the FLASH memory with the MCF5206. This is achieved by coding one PAL, U9, and connecting it as shown in Figure 6. PAL U8 is used to decode DMA signals and arbitrate the bus. The PAL equations for U8 and U9 are shown in Appendices A and B, respectively.

1.2.5 PAL Control Equations–U8

A bus arbiter is required to arbitrate between the buses of the MC68340, MCF5206 and the DMA controller. PAL U8 performs this function.

All of the logic equations assume that the system is not held in RESET and that the 68340 target hardware has the highest priority when arbitrating for the bus.

For the target hardware to assume control of the bus, BR from target hardware and BG to the DMA must be asserted.

For the MCF5206 to assume control of the bus the following conditions must be met:

Bus grant signal from the DMA controller, bus request signal from the MCF5206 and bus grant to MCF5206 must be asserted. The bus request from the MC68340 and bus grant to the 68340 must not be asserted.

A bus request signal for the DMA is created by OR'ing the two bus request signals, (MCF5206 and MC68340 bus request signals) together.

DMA is requested from the MC68340 hardware by the data request signals (either DREQ1 or DREQ2). When arbitrated off the bus the MCF5206 monitors the SIZ pins to determine the physical size of the required data transfer. The SIZx pins are driven into the correct configuration by the PAL U8.

Dynamic Bus sizing is not supported by ColdFire. The size of the data transfer is determined by the initialisation code. This code configures both chip select data size and address range as well as

DRAM data size and address range.

Appendix A illustrates all of the relevant control equations and simulation setups for coding PAL U8.

1.2.6 PAL Control Equations–U9

The 8Mbit Fujitsu MBM29F800 Flash device on the Gateway module is activated using chip select 0 (CS0) from the MCF5206. Jumper J4 multiplexes CS0 between the FLASH (CS0_ON) and the target hardware (CS0_OFF).

The control signals for the FLASH device are generated by PAL U9. These control signals consist of Write Enable (F_WE), Reset (F_RESET), Output Enable (F_OE) and Data Transfer Acknowledge (DTACK).

The generation of the DTACK signal for target hardware FLASH read/write accesses is slightly more complex than the other control signals. Two registered signals called COUNT0 and COUNT1 are created. These signals allow two wait states to be incorporated into the system for CS0_OFF and CS1. DTACK is generated from these signals.

Appendix B illustrates the corresponding set of PAL control equations for generating the FLASH and DTACK control signals.

1.3 DRAM & FLASH Memory

Figure 11 shows the connections of the on-board 1 Mbyte Fujitsu FLASH ROM (MBM29F800T) and the two blocks of EDO DRAM giving 1Mbyte of available RAM memory (MCM518160BT60).

The MCF5206 Microprocessor is connected directly to the EDO DRAM using the Column Address Strobes (CAS). CAS0, 1 are connected to the lower pictured chip and CAS 2 and 3 are connected to the upper chip in the diagram. The row address strobe 0 (RAS0) is connected to the RAS input on both chips, as is the DRAMW signal.

By connecting the RAS and CAS signals in this way to the two blocks of EDO DRAM, 1 Mbyte of EDO DRAM can be accessed using a 32-bit wide data bus.

The logic created by PAL U9 is used to drive the 1Mbyte FLASH ROM. Pull-up resistors (10K) are required for stable FLASH operation and these are connected to /BYTE and RY/BY active low pins on the chip. The pull-up resistor attached to the /BYTE pin on the FLASH device sets the operation to run in 16-bit data bus mode as opposed to the active low 8-bit setting.

Both the two EDO DRAM memory chips and the FLASH ROM chip are connected onto the main data (D0..31) and address bus (A1..21) of the MCF5206 Microprocessor.

1.4 Test Points, Decoupling and Pull-Up Resistors

Figure 10 details the key signals that can be accessed through test access points positioned on the module to aid debugging, particularly when connected to MC68340 hardware. The signals that are accessible are /TS, /AS, /DS, /DTACK, /TA, CLKOUT and R/W.

Also listed on this schematic page are the necessary signals that must be pulled-up to a high logic level to avoid false signalling. Each signal that requires a pull-up is tied to 5V using a 4.7Kohm resistor.

Jumper 5 on the schematic multiplexes BDM debug operation and JTAG operation of the MCF5206 Microprocessor. If the jumper is placed in position 2 / 3, BDM operation will be selected. Similarly, if the jumper is placed in position 1 / 2, JTAG operation will be selected.

1.5 Considerations for Implementing a MCF5206e Gateway Board

In many ways, the implementation of a MC68340 – MCF5206e Gateway board is much easier and offers higher performance due to the enhanced features of this device.

- No need for MC92310CE ASIC implementing the logic for a 2 channel DMA. The MCF5206e Microprocessor has a 2 channel DMA controller on-chip.
- Performance improvement with the MCF5206e over the MCF5206 – 50MIPS as opposed to 17MIPS!
- Maximum frequency improvement, MCF5206 has a maximum frequency of 33MHz and the MCF5206e has a maximum frequency rating of 54MHz.
- Total pin compatibility of the 160 pin MCF5206e and the MCF5206 Microprocessors.
- MCF5206e Microprocessor can handle 5V input signals, while operating from a +3.3V power supply.

Instantly, the MCF5206 Gateway reference design can be simplified by removing the circuitry surrounding the MC92310CE two channel DMA chip.

Creating a Gateway reference board for the MC68340 to the MCF5206e microprocessor would require a 3.3V supply to the MCF5206e. The easiest way to achieve this would be to have the 5V supplied from the target hardware and have it DC to DC regulated to 3.3V on the Gateway module.

After removing the circuitry for the additional port and the DMA controller from the MC68340-MCF5206 Gateway board, the PAL equations would have to be modified for the MC68340-MCF5206e Gateway board.

Again, the modifications involve removing code rather than adding it. The following equations should be removed from PAL U8 due to redundancy:

```
BR_DMA  = (BR + BR_340) * /RESET                ; OR together bus requests.

And the following equations should be modified:

BG_340  = BR_340 * BG_DMA * /BG * /RESET        ; Bus grant to the 340 H/W,

To be:

BG_340  = BR_340 * /BG * /RESET                 ; Bus grant to the 340 H/W,

And,

BG      = BR * BG_DMA * /BG_340 * (BG + /BR_340) * /RESET ; Bus grant to the 5206

To be:

BG      = BR * /BG_340 * (BG + /BR_340) * /RESET ; Bus grant to the 5206
```

The remaining schematics and logic do not need further modification for the creation of an MC68340-MCF5206e Gateway board.

It is important to note that MCF5206e operates at a maximum frequency of 54MHz. It may be necessary to modify the ColdFire initialisation code to insert additional wait states to compensate for the slower MC68340 operating frequency.

The schematic also shows the decoupling capacitors that need to be connected to all chips on the reference design to minimize the effects of noise in the system. The capacitors are connected between the power and ground planes of the module. 0.1uF and 1nF capacitors are used to inhibit both low and high frequency noise in the system.

Appendix A
PALASM Control Equations for PAL U8

```
TITLE           U8_SIGNAL_TRANSLATION
PATTERN         P00001
REVISION 1
DATE            13th September 97
AUTHOR          Pete Highton (AYL)
COMPANY         Motorola SPS (c) 1997
CHIP    U8      PALCE16V8

PIN     1       CLK  COMBINATORIAL
PIN     2       /DSACK0  COMBINATORIAL
PIN     3       /DSACK1  COMBINATORIAL
PIN     4       /BD  COMBINATORIAL
PIN     5       /RESET          COMBINATORIAL
PIN     6       /DREQ1          COMBINATORIAL
PIN     7       /DREQ2          COMBINATORIAL
PIN     8       /BR_340         COMBINATORIAL
PIN     9       /BGACK          COMBINATORIAL
PIN     10      GND
;PIN    11      NC              COMBINATORIAL
PIN     12      /BR             COMBINATORIAL
PIN     13      /BG_DMA         COMBINATORIAL
PIN     14      /BG_340         REGISTERED
PIN     15      /BG             REGISTERED
PIN     16      /DREQ           COMBINATORIAL
PIN     17      SIZ1            COMBINATORIAL
PIN     18      SIZ0            COMBINATORIAL
PIN     19      /BR_DMA         COMBINATORIAL
PIN     20      VCC
```

```
EQUATIONS
BG_340  = BR_340 * BG_DMA * /BG * /RESET  ; Bus grant to the 340 H/W,
BG_340.CLKF = CLK                          ; highest priority.

BG      = BR * BG_DMA * /BG_340 * (BG + /BR_340) * /RESET ; Bus grant to the 5206
BG.CLKF = CLK                             ; Keeps grant if already granted,
                                          ; 340 H/W has priority.
BR_DMA  = (BR + BR_340) * /RESET          ; OR together bus requests.

DREQ    = (DREQ1 + DREQ2) * /RESET        ; DREQ* from the 340 H/W

SIZ1    = BG_340 * /RESET * /DSACK0 * DSACK1   ; Dynamically size the bus for
340 H/W

SIZ0    = BG_340 * /RESET * DSACK0 * /DSACK1   ; Dynamically size the bus



;----------------------------------- Simulation Segment ------------
SIMULATION

TRACE_ON BR BG BR_340 BG_340 BG_DMA BR_DMA

SETF /BR /BR_340 /BG_DMA /RESET
CLOCKF CLK
CLOCKF CLK

SETF /BR BR_340
CLOCKF CLK
CLOCKF CLK

SETF BG_DMA
CLOCKF CLK
CLOCKF CLK

SETF BR BR_340
CLOCKF CLK
CLOCKF CLK
```

```
SETF BR /BR_340
CLOCKF CLK
CLOCKF CLK

SETF /BR /BR_340
CLOCKF CLK
CLOCKF CLK

SETF BR /BR_340
CLOCKF CLK
CLOCKF CLK

SETF BR BR_340
CLOCKF CLK
CLOCKF CLK

SETF /BR BR_340
CLOCKF CLK
CLOCKF CLK

SETF /BR /BR_340
CLOCKF CLK
CLOCKF CLK

TRACE_OFF
```

APPENDIX B
PALASM Control Equations for PAL U9

```
TITLE           U9_FLASH_DTACK
PATTERN          P00002
REVISION 1
DATE            13th September 97
AUTHOR           Pete Highton (AYL)
COMPANY         Motorola SPS (c) 1997

CHIP    U9      PALCE16V8

PIN     1       CLK             COMBINATORIAL
PIN     2       /RESET          COMBINATORIAL
PIN     3       /WR             COMBINATORIAL
PIN     4       /CS0_ON         COMBINATORIAL
PIN     5       /BY             COMBINATORIAL
PIN     6       /CS0_OFF        COMBINATORIAL
PIN     7       /CS1            COMBINATORIAL
PIN     8       /CS2            COMBINATORIAL
PIN     9       /CS3            COMBINATORIAL
PIN     10      GND
PIN     11      NC              COMBINATORIAL
PIN     12      /DSACK0         COMBINATORIAL
PIN     13      /DSACK1         COMBINATORIAL
PIN     14      /COUNT0         REGISTERED
PIN     15      /COUNT1         REGISTERED
PIN     16      /DTACK          COMBINATORIAL
PIN     17      /F_WE           COMBINATORIAL
PIN     18      /F_RESET        COMBINATORIAL
PIN     19      /F_OE           COMBINATORIAL
PIN     20      VCC
```

```
EQUATIONS


COUNT0 := (CS0_OFF + CS1) * /RESET
COUNT1 := COUNT0        ; 2 wait states for CS0 and 1


DTACK = (CS0_OFF + CS1) * (COUNT1 + (DSACK0 * /DSACK1) + (/DSACK0 * DSACK1) *
/RESET)


F_OE = /WR * CS0_ON * /BY * /RESET; FLASH output enable signal.


F_RESET = RESET * /BY   ; FLASH reset signal.


F_WE = CS0_ON * WR * /BY * /RESET; FLASH write enable signal.



;----------------------------------- Simulation Segment ------------
SIMULATION


TRACE_ON F_OE F_WE F_RESET CS0_ON WR BY RESET DTACK CS1 CS0_OFF COUNT0 COUNT1


SETF  /RESET /CS1 /CS0_OFF
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK


SETF CS1
SETF /CS1


SETF CS1
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK
SETF /CS1
```

```
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK

SETF CS0_OFF
SETF /CS0_OFF

SETF CS0_OFF
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK
SETF /CS0_OFF

SETF BY RESET /WR
CLOCKF CLK
CLOCKF CLK

SETF /BY RESET
CLOCKF CLK
CLOCKF CLK

SETF /BY /RESET
CLOCKF CLK
CLOCKF CLK

SETF CS0_ON WR
CLOCKF CLK
CLOCKF CLK

SETF /CS0_ON WR
CLOCKF CLK
CLOCKF CLK
```

```
SETF CS0_ON /WR
CLOCKF CLK
CLOCKF CLK

SETF /CS0_ON /WR
CLOCKF CLK
CLOCKF CLK

TRACE_OFF
```

Appendix C—Schematics

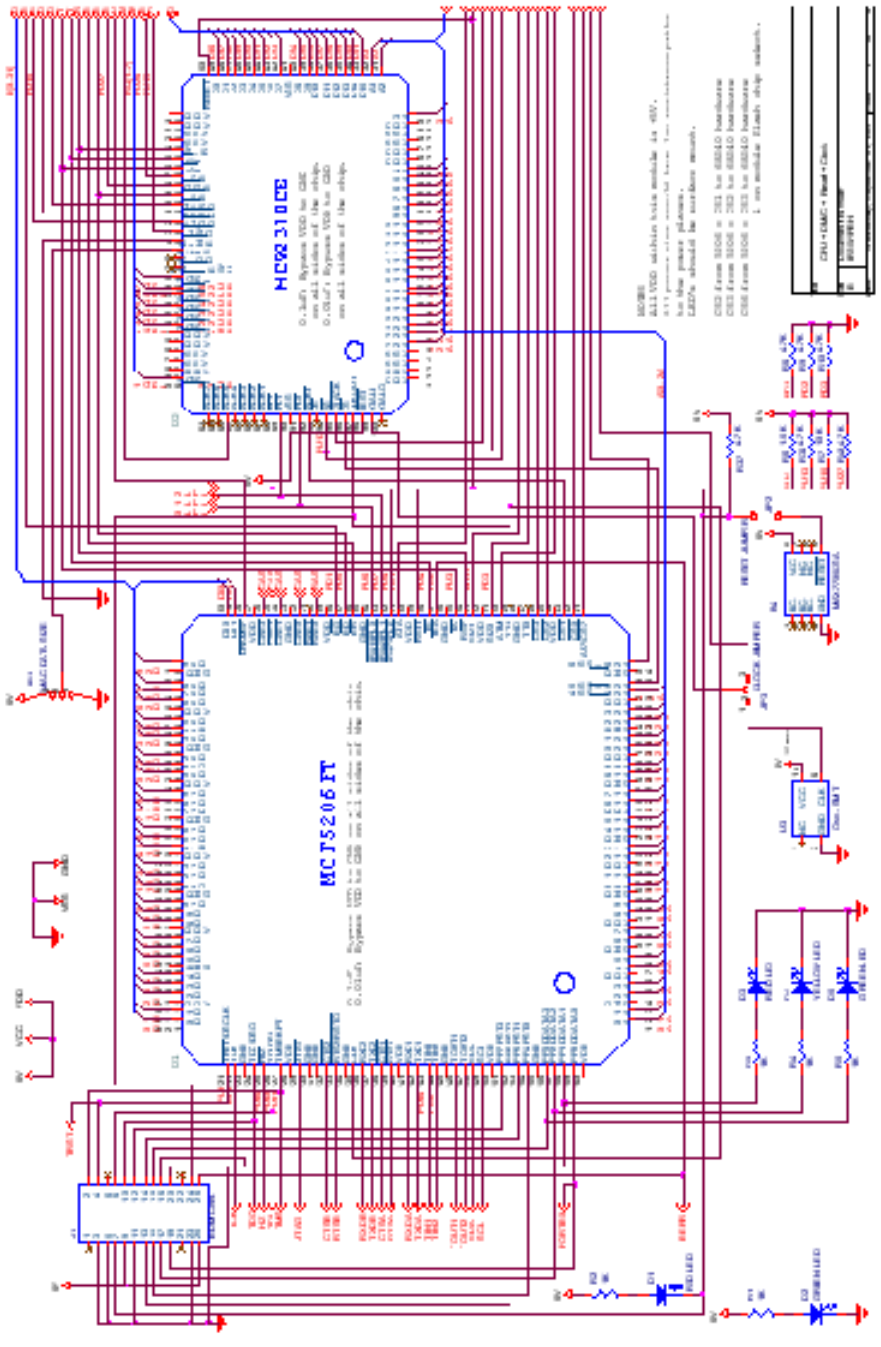

Figure 4. MCF5206 CPU, DMAC, RESET & Clock

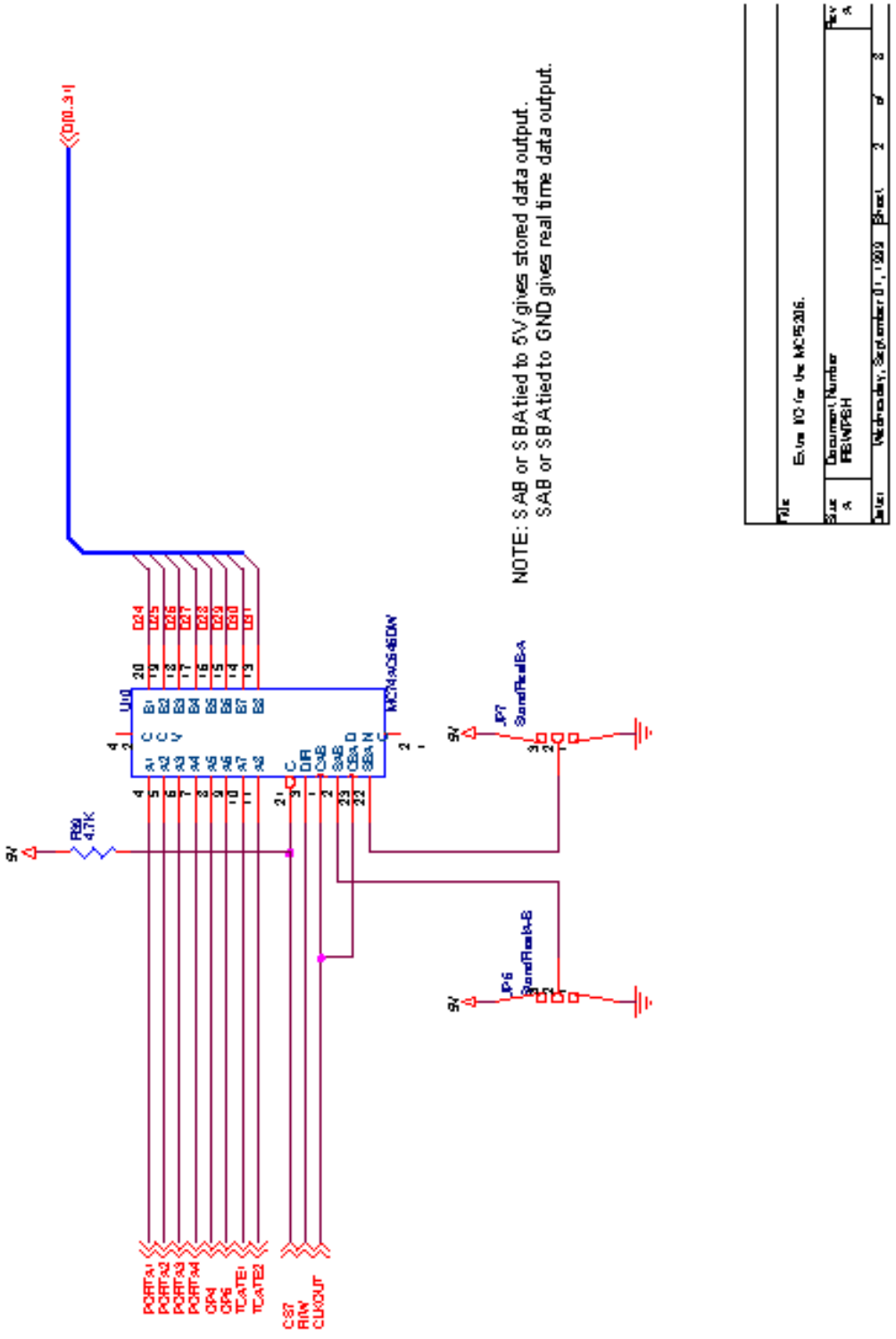

Figure 5. Extra IO for the MCF5206 Schematic

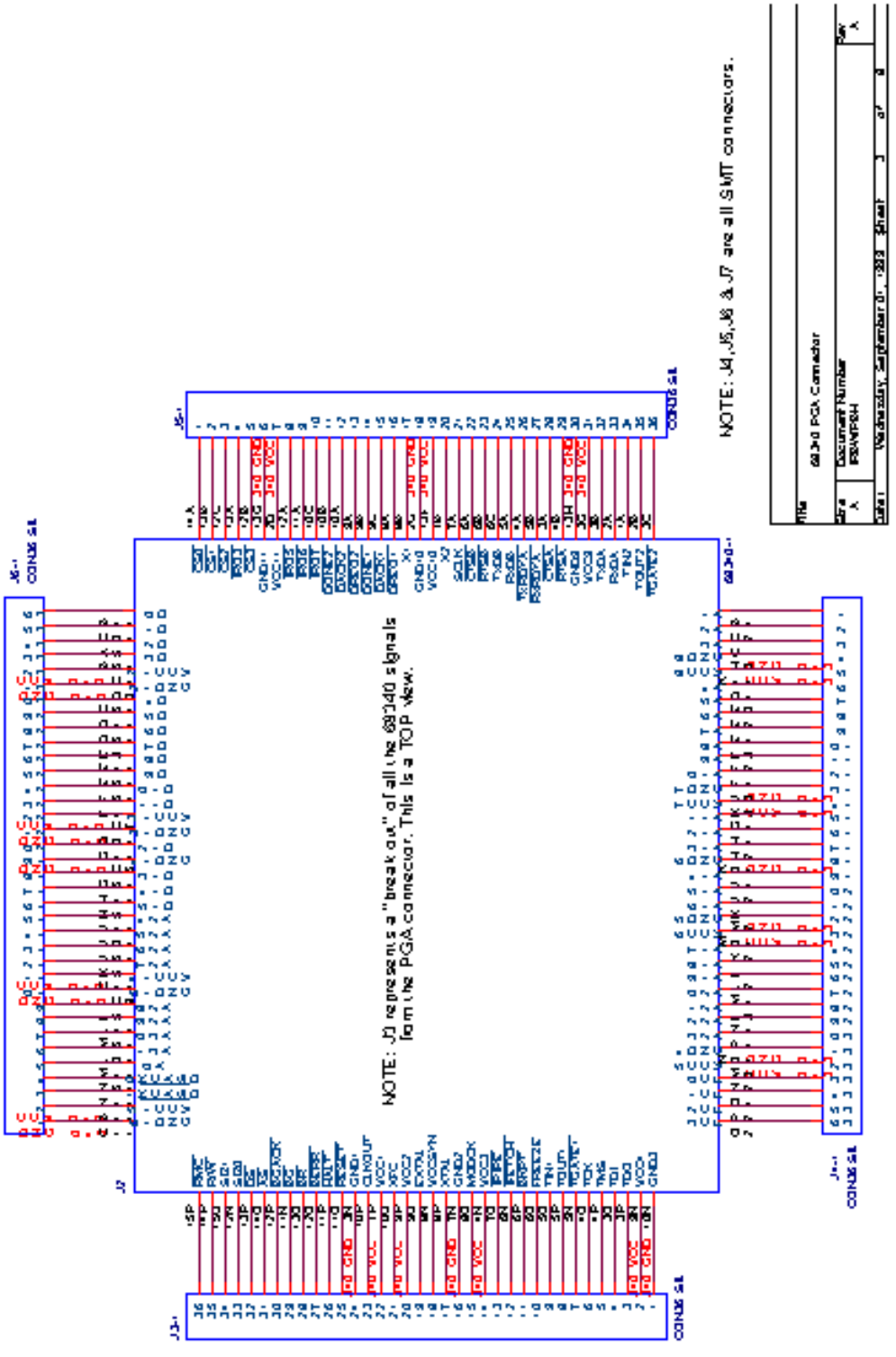

Figure 6. MC68340 PGA Footprint

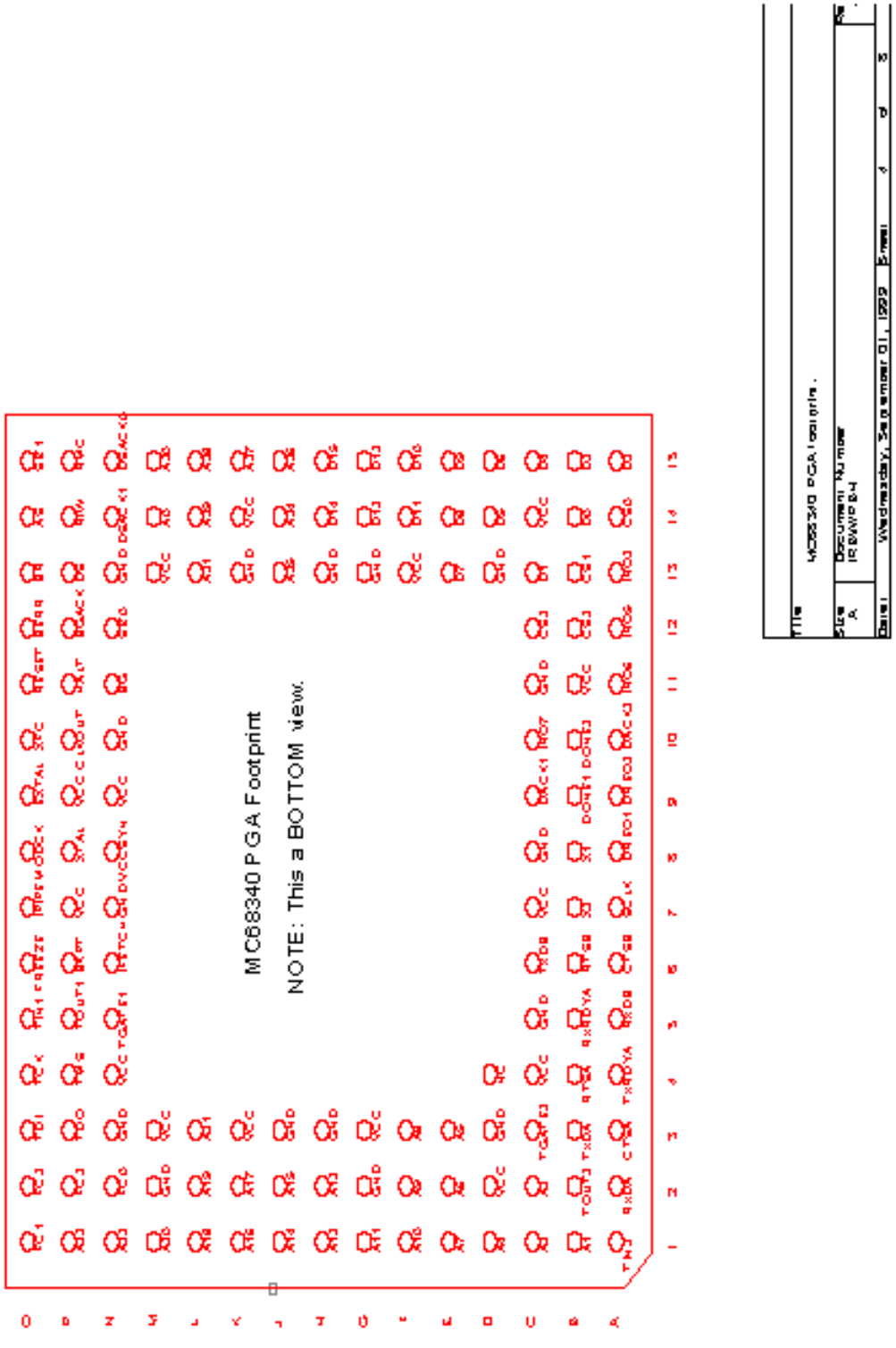

Figure 7. MC68340 PBGA Footprint Bottom View

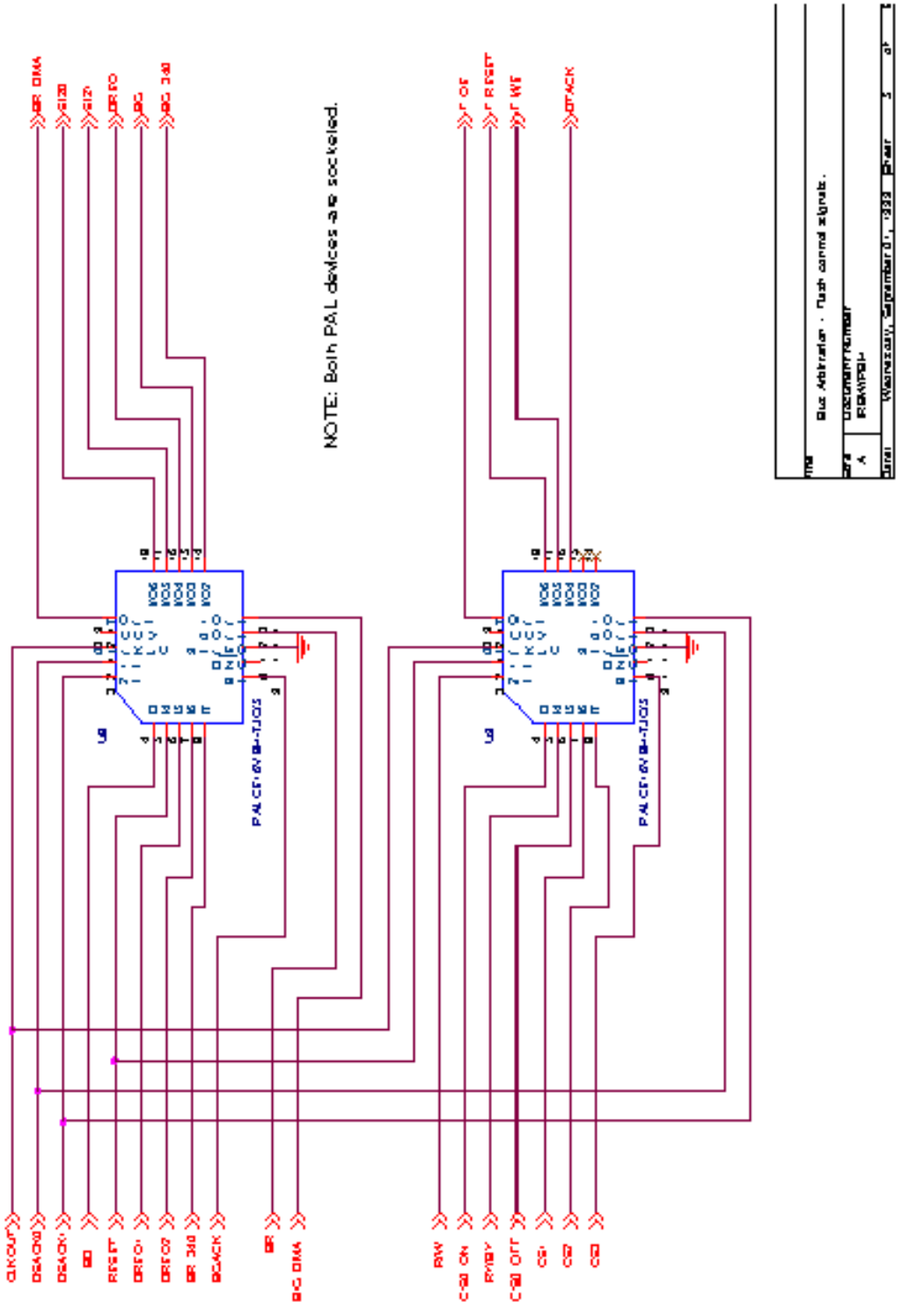

Figure 8. Bus Arbitration & FLASH Control Signals

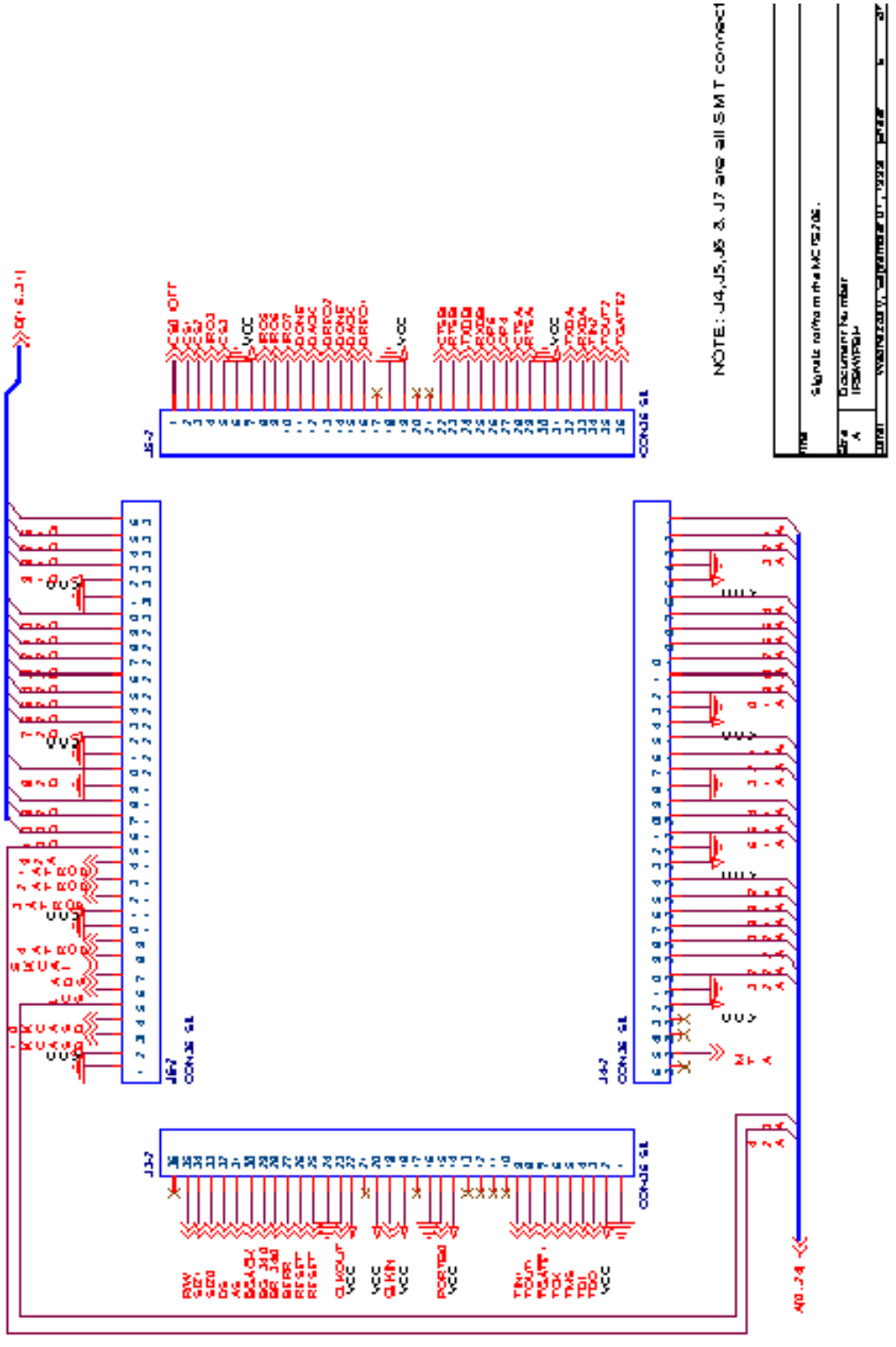

Figure 9. Signals to/from the MCF5206

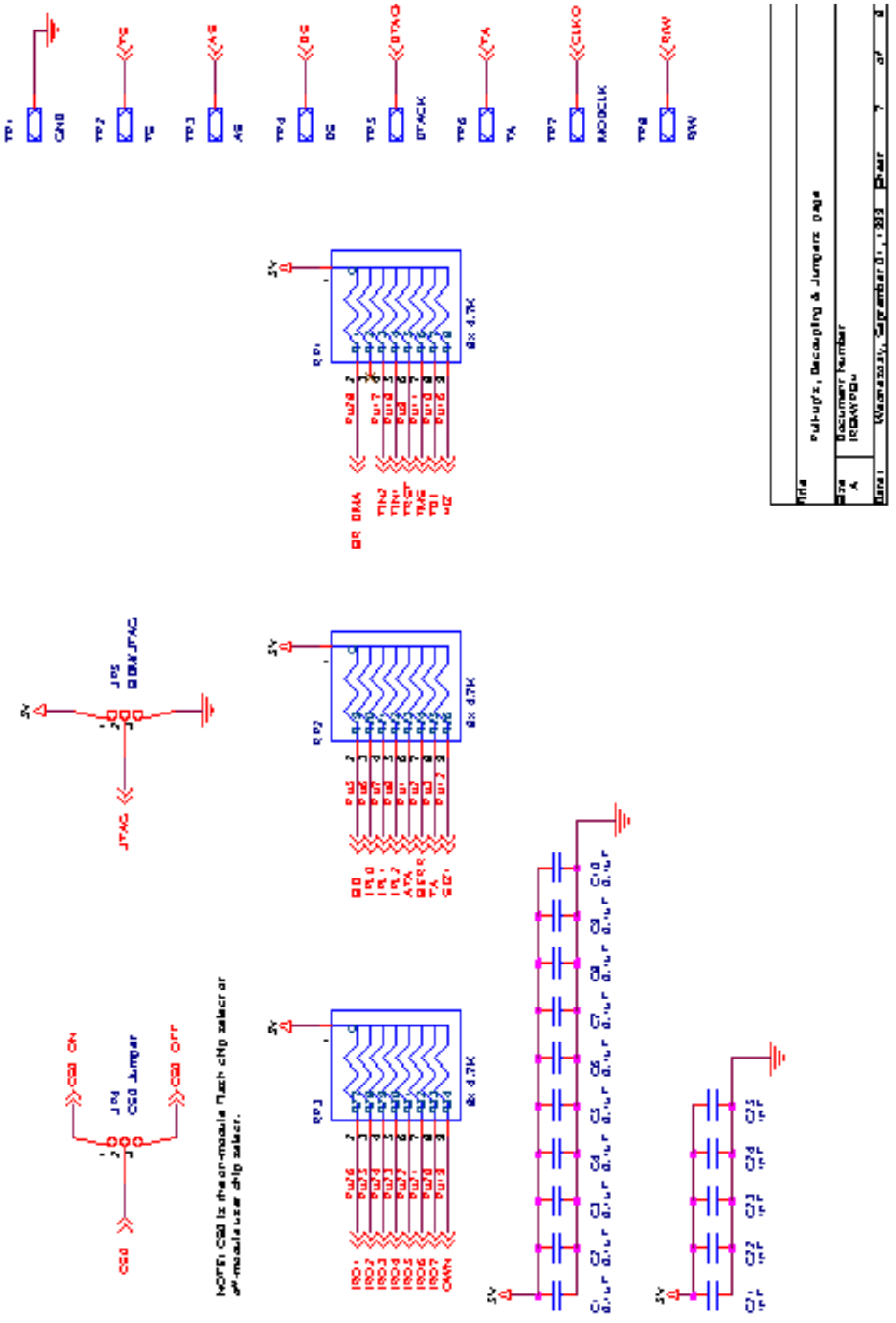

Figure 10. Pull-Ups, Decoupling and Jumpers

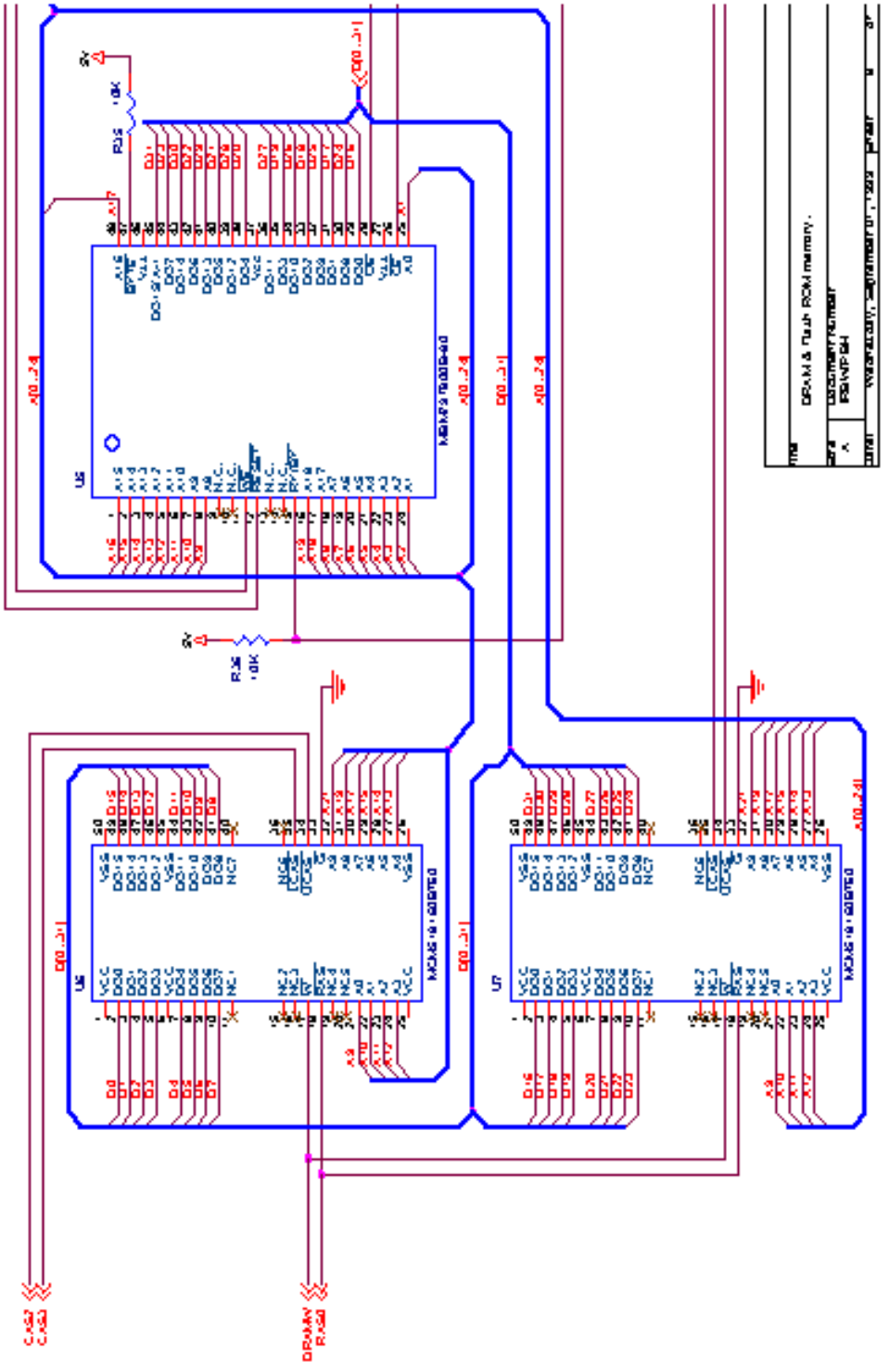

Figure 11. DRAM & FLASH Memory

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